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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 250.00 XX

Complete if Known	
Application Number	09/696,956
Filing Date	October 27, 2000
First Named Inventor	Daniel FISHER
Examiner Name	Charles CHOW
Art Unit	2618
Attorney Docket No.	001.00001

METHOD OF PAYMENT (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = _____ x Fee ($) _____ = Fee Paid ($) _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims _____ - 3 or HP = _____ x Fee ($) _____ = Fee Paid ($) _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($) _____ Fee Paid ($) _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = _____ / 50 = _____ (round up to a whole number) x Fee ($) _____ = Fee Paid ($) _____

4. OTHER FEE(S)

Fees Paid ($)

Non-English Specification, $130 fee (no small entity discount)

✓ Other (e.g., late filing surcharge): APPEAL BRIEF (Dr Small Entity) $250.00 XX

SUBMITTED BY

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PATENT APPLICATION **Attorney Docket No: 001.00001**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Daniel FISHER	)	
Serial No.: 09/696,956	)	Examiner: Charles Chow
Filed: October 27, 2001	)	Group Art Unit: 2618
For: Angle Rate Interferometer And Passive Ranger	)	

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Sir:

Responsive to the reopened prosecution Office Action dated August 9, 2006, appellant submits this Appeal Brief in furtherance of the Notice of Appeal filed by mail under Rule 8 on June 7, 2006 with regard to the above identified patent application and a second Notice Of Appeal filed herewith. The fee for the Notice of Appeal was paid when the June 7 Notice Of Appeal was filed. Concurrently herewith is attached a renewed Notice Of Appeal, but the Notice Of Appeal fee was already paid on June 7 (35 U.S.C. §134(a) provides that "An applicant for patent ... may appeal ... having once paid the fee for such appeal."). Attached hereto is the Appeal Brief fee under 37 C.F.R. §41.20(b)(2) for a small entity, currently $250.00. This case is ripe for appeal since it has been pending over six years, and during that time, the Patent Office Action has issued at least five Office Action rejecting one or more claims.

Appellant further notes that this Appeal Brief is being transmitted, pursuant to 37 C.F.R. § 41.37(a), and the structure of this Brief is as follows and in the order required by 37 C.F.R.§ 41.37(c):

I. Real Party in Interest
II. Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection
VII. Arguments
VIII. Claims Appendix
IX. Evidence Appendix
X. Related Proceedings.

I. Real Party in Interest (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest with respect to the present appeal is the inventor.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

None.

III. Status of Claims (37 C.F.R. § 41.37(c)(1)(iii))

Claim 1-15 and 17-21 and 23-29 are currently pending. It is the final rejections of claims 1-2, 9, 14-15, 24-25 and 27, as set forth in the Claims Appendix, that are appealed. The Office Action objects to claims 10-13, 26 and 29 asserting that these claims depend on a rejected base claim; however, as discussed herein, the Applicant asserts that the base claims, upon which claims 10-13, 26 and 29 depend, are allowable.

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

No Amendment has been filed subsequent to the final rejection.

V. Summary of the Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

The subject matter of the present invention is a passive receiver (no transmitter) with an RF bridge and a processor (see FIGS. 1 and 2). One example of the RF bridge is depicted in FIG. 3. One example of the processor is depicted in FIG. 4. The RF bridge and the processor cooperate to measure an angle rate (i.e., a rate of change of a bearing angle) to a non-cooperating emitter, and with the measured angle rate, compute a range to the non-cooperating emitter. In particular, the RF bridge and the processor cooperate to measure an angle rate and compute the range in a short time interval (e.g., a few hundred milliseconds) with useful range accuracies, for example 20% of range (see the specification in general, e.g., page 1, line 4 through page 2, line 2 and page 17, line 18 through page 24, line 9).

With regard to a first embodiment, typical of independent claim 1, a receiver (see FIG. 1) includes a processor 200 and an RF bridge 100 coupled to the processor to receive a reference signal 202 from the processor. Alternatively, a receiver (see FIG. 2) includes a processor 200 and an RF bridge 100 coupled to the processor to receive a reference signal 302 from the processor. In FIG. 3, RF bridge 100 includes first and second frequency converters 140, 160 coupled to respective first and second antennas 104, 102, and a third frequency converter 180 coupled to outputs of the first and second frequency converters. The claimed structure is disclosed generally throughout the specification, for example in page 3, line 25 through page 9, line 24. In particular, as disclosed in the specification, at page 25, lines 19-24, an embodiment of "a receiver includes processor 200 and RF bridge 100. RF bridge 100 is coupled to processor 200 to receive reference signal 202 or intermediate reference signal 302. RF bridge 100 includes first and second frequency converters 140 and 160 coupled to respective first and second

antennas 104 and 102. RF bridge 100 also includes third frequency converter 180 coupled to outputs of the first and second frequency converters 140 and 160."

The specification also discloses that the reference signal 202 is characterized by a constant predetermined frequency. As disclosed in the specification, at page 6, lines 21-24, "reference signal 202 [is] preferably spectrally pure. Typically, the frequency of processor reference signal 202 is based on a direct digital synthesizer, a frequency multiplied replica of a crystal oscillator, or a phase locked loop synthesizer." A spectrally pure reference signal is inherently a reference signal that is characterized by a constant predetermined frequency. As disclosed in the pending specification, at page 9, lines 25-28, "processor 200 includes digital frequency source 206 and digital to analog converter 208 (DAC 208) to produce processor reference signal 202. Collectively, frequency source 206 and DAC 208 constitute a direct digital synthesizer. In the examples discussed above, processor reference signal 202 is a spectrally pure 8 MHz signal."

With regard to a first variant of the above described first embodiment, typical of claim 2 dependent on claim 1, and as depicted in FIGS. 1-3, the third frequency converter180 provides an information signal 204 that is coupled to the processor 200. The claimed structure is disclosed generally throughout the specification, for example in page 3, line 25 through page 9, line 24. In particular, as disclosed in FIG. 1 and the specification at page 4, lines 11-14, "RF bridge 100 produces an information signal ... [and] processor 200 receives the information signal as processor input signal 204." Also, as disclosed in FIG. 3 and the specification at page 6, lines 5-14, "mixer 180 ... produces the lower sideband mixer result ... [that is filtered] by filter 190 to provide the information signal from RF bridge 100." Furthermore, as disclosed in FIG. 3 and in the specification at page 6, lines 17-19, "outputs of filters 150 and 170 are mixed in mixer 180 and filtered in filter 190. The output of filter 190 is the information signal applied as processor input signal 204."

With regard to a second variant of the above described first embodiment, typical of claim 24 dependent on claim 1, and as depicted in FIGS. 1-3, the reference signal 202 is coupled to only one of the first and second frequency converters 140, 160. As depicted in FIG. 3, the reference signal from the processor is coupled through mixer 120 and filter 130 to frequency converter 140. In FIG. 3, the reference signal 202 is coupled to second frequency converter 140, but not first frequency converter 160 since the direction of the signal from frequency source 110 to frequency converter 120 would preclude reference signal 202 from reaching first frequency converter 160. The claimed structure is disclosed generally throughout the specification, for example in page 5, lines 9-21.

With regard to a second embodiment typical of independent claim 25 and similar to the discussion above with respect to claim 1, a receiver (see FIG. 1) includes a processor 200 and an RF bridge 100 coupled to the processor to receive a reference signal 202 from the processor. Alternatively, a receiver (see FIG. 2) includes a processor 200 and an RF bridge 100 coupled to the processor to receive a reference signal 302 from the processor. In FIG. 3, RF bridge 100 includes first and second frequency converters 140, 160 coupled to respective first and second

antennas 104, 102, and a third frequency converter 180 coupled to outputs of the first and second frequency converters.

Unlike claim 1, claim 25 is not limited to a reference signal is characterized by a constant predetermined frequency. Instead, in claim 25, the reference signal 202 is coupled to only one of the first and second frequency converters 140, 160 as discussed above with respect to claim 24. As depicted in FIG. 3, the reference signal from the processor is coupled through mixer 120 and filter 130 to frequency converter 140. In FIG. 3, the reference signal 202 is coupled to second frequency converter 140, but not first frequency converter 160 since the direction of the signal from frequency source 110 to frequency converter 120 would preclude reference signal 202 from reaching first frequency converter 160. The claimed structure is disclosed generally throughout the specification, for example in page 5, lines 9-21.

With regard to a third embodiment typical of independent claim 9, a receiver (see FIG. 1 or 2) includes an RF bridge 100 and a processor 200 coupled to the RF bridge to receive an information signal 204 from the RF bridge. In FIG. 4, the processor 200 includes a digital frequency source 206 to generate a reference signal 202 based on a signal from a clock source. In FIG. 1 (or FIG. 2), the reference signal 202 (or 302) is coupled to the RF bridge 100. Processor 200 further includes circuitry to detect (circuit parts 230, 240, 260, 270 and 280 of FIG. 4) a frequency difference from the information signal 204 based on the signal from the clock source. The claimed structure is disclosed generally throughout the specification, for example in page 3, line 25 through page 9, line 24. In particular, as disclosed in the specification at page 26, line 25 through page 27, line 2, an alternative embodiment of "a receiver includes RF bridge 100 and processor 200 coupled to the RF bridge to receive information signal 204 [see FIG. 1] from the RF bridge. The processor includes a central clock source (not shown but common in digital designs), digital frequency source 206 to generate reference signal 202 based on a signal from the clock source, and reference signal 202 coupled to RF bridge 100. The processor further includes circuitry to detect a frequency difference from the information signal based on the signal from the clock source (e.g., circuit parts 230, 240, 260, 270 and 280 of FIG. 4)." Also, as disclosed in the specification at page 9, lines 25-27, "processor 200 includes digital frequency source 206 and digital to analog converter 208 (DAC 208) to produce processor reference signal 202. Collectively, frequency source 206 and DAC 208 constitute a direct digital synthesizer."

With regard to a variant of the above described third embodiment, typical of claim 14 dependent on claim 9, and as depicted in FIGS. 1-3, RF bridge 100 includes first and second RF frequency converters 140, 160 coupled to respective first and second antennas 104, 102, and a third RF frequency converter 180 coupled to outputs of the first and second RF frequency converters. The claimed structure is disclosed generally throughout the specification, for example in page 3, line 25 through page 9, line 24. In particular, as disclosed in FIG. 3 and the specification at page 5, line 9-10, "RF bridge 100 includes ... mixers ... 140, 160 and 180 and filters ... 150, 170 and 190." As disclosed in FIG. 3 and the specification at page 5, line 26-27, "Mixer 160 and filter 170 produce a signal that is a frequency shifted replica of the emitter signal received at antenna 102." As disclosed in FIG. 3 and the specification at page 6, line 1-2, "Mixer 140 and filter 150 produce a signal that is a frequency shifted replica of the emitter signal

received at antenna 104." As disclosed in FIG. 3 and the specification at page 6, line 5-9, "The signals from filters 150 and 170 are then combined in mixer 180... [coupled through filter 190] to provide the information signal from RF bridge 100."

With regard to an example of the above described variant of the above described third embodiment, typical of claim 15 dependent on claim 14, and as depicted in FIGS. 1-3, the first and second RF frequency converters 140, 160 receive respective first and second signals from the respective first and second antennas 104, 102. The third RF frequency converter 180 heterodynes signals from the first and second RF frequency converters 140, 160 to provide a signal that is characterized by a frequency difference modulated onto the reference signal. The frequency difference is a difference between a frequency of the first signal and a frequency of the second signal. The claimed structure is disclosed generally throughout the specification, for example in page 3, line 25 through page 9, line 24 and page 26, lines 1-6. In particular, as disclosed in FIG. 3 and the specification at page 5, line 9 through page 7, line 11 and on page 26, lines 1-6, "the first and second frequency converters 140 and 160 receive respective first and second signals from the respective first and second antennas 104, 102. The third frequency converter 180 heterodynes signals from the first and second frequency converters 140 and 160 to provide a signal that is characterized by a frequency difference modulated onto the reference signal. The frequency difference is a difference between a frequency of the first signal and a frequency of the second signal."

With regard to a fourth embodiment, typical of independent claim 27, a receiver (see FIG. 1 or 2) includes an RF bridge 100 and a processor 200 coupled to the RF bridge to receive an information signal 204 from the RF bridge. In FIG. 4, the processor 200 includes a digital frequency source 206 to generate a reference signal 202 based on a signal from a clock source. In FIG. 1 (or FIG. 2), the reference signal 202 (or 302) is coupled to the RF bridge 100. Processor 200 further includes circuitry to detect (circuit parts 230, 240, 260, 270 and 280 of FIG. 4) a frequency difference from the information signal 204 using the signal from the clock source. The claimed structure is disclosed generally throughout the specification, for example in page 3, line 25 through page 9, line 24. In particular, as disclosed in the specification at page 26, line 25 through page 27, line 2, an alternative embodiment of "a receiver includes RF bridge 100 and processor 200 coupled to the RF bridge to receive information signal 204 [see FIG. 1] from the RF bridge. The processor includes a central clock source (not shown but common in digital designs), digital frequency source 206 to generate reference signal 202 based on a signal from the clock source, and reference signal 202 coupled to RF bridge 100. The processor further includes circuitry to detect a frequency difference from the information signal based on the signal from the clock source (e.g., circuit parts 230, 240, 260, 270 and 280 of FIG. 4)." Also, as disclosed in the specification at page 9, lines 25-27, "processor 200 includes digital frequency source 206 and digital to analog converter 208 (DAC 208) to produce processor reference signal 202. Collectively, frequency source 206 and DAC 208 constitute a direct digital synthesizer."

The only difference between claim 27 and claim 9 is that claim 27 specifies "circuitry to detect a frequency difference from the information signal <u>using</u> the signal from the clock source" and claim 9 specifies "circuitry to detect a frequency difference from the information signal <u>based on</u> the signal from the clock source" (emphasis added to show the difference.

VI. Grounds of Rejection To Be Reviewed on Appeal (37 C.F.R. § 41.37(c)(1)(vi))

Ground A. Whether any one or all of claims 1-2, 9, 14-15, 24, 27 are unpatentable under 35 U.S.C. 103(a) over U.S. Patent No. 3,816,834 to Wilson in view of U.S. Patent No. 4,893,316 to Janc et al. (hereinafter, Janc) and U.S. Patent No. 6,268,829 to Weckstrom.

Ground B. Whether claim 25 is unpatentable under 35 U.S.C. 103(a) over U.S. Patent No. 3,816,834 to Wilson in view of U.S. Patent No. 6,268,829 to Weckstrom.

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

A. Claims 1-2, 9, 14-15, 24, 27 Are Not Rendered Unpatentable Under 35 U.S.C. 103(a) For Being Obvious Over Wilson In View Of Janc et al. And Weckstrom.

The Office Action rejects claims 1-2, 9, 14-15, 24, 27 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 3,816,834 to Wilson in view of U.S. Patent No. 4,893,316 to Janc et al. (hereinafter, Janc) and U.S. Patent No. 6,268,829 to Weckstrom. This rejection is respectfully traversed.

The Office Action fails to establish a *prima facie* case that independent claims 1, 9 and 27, and claims dependent thereon, would have been obvious to a person of ordinary skill in the art at the time of the invention. The United States Supreme Court established the basic rules for analyzing an invention's obviousness and articulated three factual inquiries to be made in an obviousness determination. *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). This analysis requires a factual inquiry into (1) the scope and content of the prior art, (2) the differences between the prior art and the claimed subject matter, and (3) the level of skill of a person of ordinary skill in the art at the time the invention was made. The M.P.E.P. instructs that "examiners should apply the test for patentability under 35 U.S.C. §103 set forth in *Graham*." See M.P.E.P. 2141 through 2143.

The determination of obviousness under 35 U.S.C. §103(a) is a legal conclusion that must be based on factual evidence. *Burlington Indus., Inc. v. Quigg*, 822 F.2d 1581, 1584, 3 USPQ2d 1436, 1439 (Fed. Cir. 1987). The results of the factual inquires articulated in *Graham v. John Deere Co.* provide the factual evidence upon which the legal conclusion of obviousness is to be based. Furthermore, the U.S. Patent and Trademark Office bears the initial burden of establishing that the claimed invention is *prima facie* obvious. *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). M.P.E.P. 4142 instructs that the "examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness."

It is respectfully submitted that the Office Action fails to support a legal conclusion of obviousness with factual evidence that the applied references combined would achieve the claimed invention, or that the asserted motivation to combine the applied references is disclosed in the applied references. This rejection will be traversed in numbered sections as follows.

1. Janc is non-analogous art
2. Claim 1
3. Claim 2 (dependent on claim 1)
4. Claim 24 (dependent on claim 1)
5. Claims 9 and 14-15 (dependent on claim 9) and claim 27

1. Janc Is Non-Analogous Art

M.P.E.P. §2141.01(a) instructs that, to be analogous, a reference must either be in the field of the applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned. "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of the applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992).

a. Field Of Janc's Endeavor

At the outset, it must be recognized that Janc is concerned with radio communications substantially implemented in digital circuitry and not with a passive receiver (without a transmitter) that determines the angle rate of, and the range to, a non-cooperating emitter.

The M.P.E.P., e.g. §2141.01(a), gives guidance, in the form of an exemplary case, on what constitutes non-analogous art and how the Federal Circuit determines "same field of endeavor" in another electronics case. A reference does not become analogous art to the patent claims, merely because the reference, like the claimed invention, dealt with single inline memory modules (SIMMs). See *Wang Laboratories, Inc. v. Toshiba Corp.*, 993 F.2d 858, 26 USPQ2d 1767 (Fed. Cir. 1993). In the *Wang* case, the patent claims dealt with SIMMs for installation on a printed circuit motherboard for use in a personal computer. In the *Wang* case, the reference dealt with SIMMS used in an industrial controller. The reference was found to be in a different field of endeavor because it involved memory circuits in which modules of varying sizes may be added or replaced in an industrial controller, whereas the claimed invention in the patent involved compact modular memories for a personal computer.

Janc is not concerned with the same field of endeavor as the present invention. The field of endeavor of Janc's patent is that of "radio communications and specifically to a radio frequency receiver which is substantially implemented with digital circuitry" (see Janc's column 1, lines 10-13). Janc has nothing to do with measuring angles, angle rates or range. In contrast, the field of endeavor of the present invention is that of a passive receiver (without a transmitter) that determines the angle rate of, and the range to, a non-cooperating emitter (see the present specification generally, e.g., page 2, lines 7-9).

Note that the applicant's field of endeavor cannot be radio communications (as in Janc) at least because any communication signal that may or may not have been modulated on a

communication carrier signal from a non-cooperating emitter (i.e., a source of radiation) is cancelled by the very structure of the presently claimed receiver.

The present specification generally (e.g., page 4, lines 3-13, with reference to FIG. 1) discloses how RF bridge 100 receives a signal from an emitter, discloses that baseline 106 between antennas 102 and 104 rotates with respect to a line of sight to the emitter producing a frequency difference proportional to an angle rate of rotation, and RF bridge 100 produces an information signal that has the frequency difference frequency modulated on a reference signal 202. Since the signal from the distant emitter is cancelled within the RF bridge, and only the rate of rotation of baseline 106 is provided by the RF bridge (in the form of an information signal), the applicant's field of endeavor cannot be radio communications.

Similarly, the present specification generally (e.g., page 5, line 26 through page 6, line 20 with reference to FIG. 3) discloses how the outputs of mixers 140 and 160 are combined in mixer 180 to produce a lower sideband signal, thus any signal commonly received on both antennas 102 and 104 would be cancelled. This cancellation property applies not only to communication signals that may be modulated onto a carrier signal, but also to the carrier signal itself. In fact, a specific example is disclosed where the emitter signal is a TV channel 2 signal yet the information signal produced out of mixer 180 includes a frequency difference up to 1 Hertz (due to a rotating baseline 106 of FIG. 1) modulated onto an 8 MHz reference signal 202 without any residue of the TV signal. A communication signal would simply be cancelled within RF bridge 100. Other specific examples are also discussed (e.g., page 7, lines 12-26). The applicant's field of endeavor cannot be radio communications at least because the RF bridge cannot provide a communication signal output because of the very structure of the presently claimed receiver.

The present specification (e.g. page 26, lines 1-6) discloses that frequency converter 180 heterodynes signals from frequency converters 140 and 160 to provide an information signal characterized by a frequency difference modulated onto the reference signal. Again, the applicant's field of endeavor cannot be radio communications at least because the RF bridge cannot provide a communication signal output because of the very structure of the presently claimed receiver.

b. Janc Not Pertinent to Problem Of Inventor's Concern

Furthermore, Janc is not reasonably pertinent to the particular problem with which the present inventor was concerned. "A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem," or at least so say the Federal Circuit in *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992).

The particular problem addressed by Janc's patent is the elimination of "undesirable variations in those operations which may have resulted from external effects such as temperature, humidity, and aging of analog components" (see Janc's column 1, lines 26-29). In contrast, the particular problem with which the present inventor was concerned is the measurement of a range

to a non-cooperating emitter using only a passive receiver with no active transmitter, and in particular, the measurement of the range in a short time interval (e.g., a few hundred milliseconds) with useful range accuracies, for example 20% of range (see the specification in general, e.g., page 1, line 4 through page 2, line 2 and page 17, line 18 through page 24, line 9).

Janc's subject matter is not one that logically would have commended itself to an inventor's attention when an inventor is considering the problem of measuring a range to a non-cooperating emitter. Janc simply addresses a different problem from that of the present application. The Office Action fails to cite any evidence, or even assert reasoned argument, that Janc's solution to the problem of eliminating "undesirable variations in those operations which may have resulted from external effects such as temperature, humidity, and aging of analog components" (i.e., the problem of Janc's concern) would logically have commended itself to an inventor's attention in considering the problem of measuring a range to a non-cooperating emitter.

The Office Action's citation of Janc is an exercise in hindsight. The present application discloses at page 6, lines 22-24, "the frequency of processor reference signal 202 is based on a direct digital synthesizer, a frequency multiplied replica of a crystal oscillator, or a phase locked loop synthesizer" and at page 9, lines 26-27 "frequency source 206 and DAC 208 constitute a direct digital synthesizer." It is hindsight to use the application's disclosure of a DDS to identify the DDS as an element to search for, particularly in non-analogous art. Only hindsight could twist the meaning of "logically would have commended itself to an inventor's attention" (as cited from *In re Clay*) so far as to make one seeking to measure a range somehow look to the art of digital implementations to overcome variations in analog components in communication systems.

c. Conclusion: Janc Is Non-Analogous Art

Janc is neither "in the field of the applicant's endeavor" nor "reasonably pertinent to the particular problem with which the inventor was concerned" as required of an analogous art reference according to M.P.E.P. §2141.01(a). For at least this reason, withdrawal of all rejections that use Janc as a prior art reference is earnestly solicited.

2. Claim 1 Is Not Rendered Obvious By The Applied Art

Even if, *arguendo*, Janc was to be regarded as analogous art to the subject matter of the present application, the proposed combination does not achieve the claimed invention and the Office Action still fails to establish a *prima facie* case that claim 1 would have been obvious to a person of ordinary skill in the art at the time of the invention.

To establish a *prima facie* case of obviousness, the Patent and Trademark Office must demonstrate by substantial evidence that the prior art relied upon, coupled with the knowledge generally available in the art that the time of the invention, contains some suggestion or incentive that would have motivated an ordinarily skilled person to modify the subject matter of a reference or combine the subject matters of the references to achieve the claimed subject matter.

In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). M.P.E.P. 2143.01 instructs that "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art."

Wilson in view of Janc and Weckstrom does not disclose, teach or suggest a receiver:

> comprising a processor and an RF bridge coupled to the processor to receive a reference signal from the processor, the reference signal being characterized by a constant predetermined frequency,

as specified in claim 1, and therefore as contained in claims 2 and 24 dependent on claim 1.

a. Clarifying Terms And Phrases Used In The Office Action.

Several assertions in the Office Actions are either unclearly articulated or clearly in error. In order for responses to be clear, several terms and phrases must be unambiguously interpreted.

i. First, the Office Action's assertions with respect to Wilson's "processing circuitry" are interpreted to mean analog processing circuitry. The Office Action, on page 2, lines 14-15, asserts that Wilson teaches a receiver "comprising a processing circuitry for producing a reference signal [18, 24, 26, 22, 35]" (brackets in original). The meaning of "processing circuitry" is predicate to an understanding the Office Action's interpretation of Wilson and interpretation of the relationship of Wilson to Janc and Weckstrom. Although ambiguous, a fair reading of the Office Action as a whole reveals that the Office Action is not attempting to assert that the "processing circuitry" of Wilson is digital. Certainly, the disclosure of Wilson would not even suggest to a person of ordinary skill that the "processing circuitry" of Wilson is digital.

For example, the Office Action later admits that Wilson & Janc fail to teach placing the processing circuitry into a processor (page 3, line 5) and asserts that Weckstrom teaches "control unit 88 ... for processing the information signal ... " (page 3, lines 6-8). Then, the Office Action asserts that "it would have been obvious to place" Wilson's analog "components 18, 22, 24, 24, 35 [i.e., processing circuitry] into the processor of Wilson & Janc that produces the references signal" (see page 3, line 9-11). Whereas Wilson's components are analog components, the Office Action is read as asserting some part of Janc's circuitry is digital and constitutes at least a part of the processor that produces the claimed reference signal. See below for a searching inquiry into what the Office Action believes to be the processor of Janc.

The Office Action's assertion on page 3, lines 9-11 that the analog components 18, 22, 24, 24, 35 of Wilson are placed "into the processor of Wilson & Janc" is unclear. For purposes of this response; however, the Office Action's assertions on page 3, lines 6-9 are interpreted to mean that Weckstrom's control unit 88, not any part of Janc, is the processor that receives the claimed information signal. Thus, there are two processors. If the Patent Office means to assert

to the contrary or that Wilson's "processing circuitry" is to be read as digital, the Patent Office is invited to clarify its position in its next responsive communication.

ii. Second, the Office Action's assertion with respect to Wilson producing a reference signal is interpreted to mean that the signal from Wilson's low frequency oscillator 18 is to be read as a reference signal. The Office Action, on page 2, lines 17-18, asserts that the RF bridge is coupled "the processing circuitry [18, 24, 26, 22, 35] to receive a reference signals from processing circuitry [receiving 1 MHz reference signal from oscillator 18]" (brackets in original). This can best be construed to mean that the Office Action asserts that the 1 MHz signal output of Wilson's low frequency oscillator 18 is to be read as the claimed reference signal. If the Patent Office means to assert to the contrary, the Patent Office is invited to clarify its position in its next responsive communication.

iii. Third, the Office Action's assertion on page 4 with respect to Janc's element 1976 is incorrect. On page 4, lines 9-11 in the section discussing claims 9 and 27, the Office Action asserts that Janc's "1920 includes a digital source generator 1976," that digital source generator 1976 is also known as LO 626 in FIG. 6, and that this digital source generator is "to generate reference quadrature signal from clock source 1934." This assertion is respectfully traversed.

It is regrettable and confusing that FIG. 19 has two features labeled 1976. FIG. 19 correctly labels a pre-selector with numeral 1976 (see column 20, lines 18-26) and incorrectly labels the digital quadrature local oscillator as numeral 1976. The digital quadrature local oscillator in FIG. 19 should have been labeled 1926. Support for this labeling correction is found in the text of Janc. Janc discloses that like reference numerals identify like elements (see column 5, lines 31-34). In the case of the digital quadrature local oscillator, this feature is labeled 426 in FIG. 4, labeled 526 in FIG. 5, and labeled 2026 in FIG. 20. It logically follows that this feature should be labeled 1926 in FIG. 19. Janc discloses that "FIG. 6 is a block diagram of the digital quadrature LO of FIGS. 4 and 5" (column 5, lines 47-48), and FIG. 6 is labeled, as a whole, digital quadrature local oscillator as 626. Also see column 11, lines 1-2. The digital quadrature local oscillator in FIG. 19 should have been labeled 1926.

With a corrected view of Janc's disclosure, Janc actually discloses that digital quadrature LO 626 (or 426, or 526, or 1926, or 2026) is a direct digital synthesizer (DDS) that is coupled to a pair of digital mixers (422, 424 of FIG. 4 or 522, 524 of FIG. 5 or 1922, 1924 of FIG. 19 or 2022, 2024 of FIG. 20) in a digital zero-IF selectivity section that Janc refers to as a DZISS. Janc's DZISS is a digital counterpart to an analog down converter that converts an incoming signal to base band (see Janc column 10, lines 26-29). Also, such a DZISS, with little modification, can be used as a digital up converter to convert a base band signal to some carrier frequency (see Janc column 10, lines 45-47 and 53-59).

Digital quadrature LO 626 (or 426, or 526, or 1926) functions as a local oscillator within the DZISS. The pair of digital mixers (422, 424 of FIG. 4 or 522, 524 of FIG. 5 or 1922, 1924 of FIG. 19 or 2022, 2024 of FIG. 20) functions to down convert (or up convert) the incoming signal. The two digital low pass filters (432, 432' of FIG. 4, 532, 532' of FIG. 5, 1932, 1932' of

FIG. 19 and 2032, 2032' of FIG. 20) filter out all but the base band signals from the output of the digital mixers (FIGS. 4 and 19) or the input to the digital mixers (FIGS. 5 and 20). For down converters, these digital filters function to eliminate the high heterodyned frequency that may be output from the mixers. In up converters, these digital filters function as anti-alias filters to ensure that only base band signals are mixed with the local oscillator frequency.

b. What Part Of Janc's Disclosure Is To Be Regarded As The Processor?

The Office Action's assertions are ambiguous as to what part of Janc's disclosed circuitry is to be regarded as the claimed "processor." On page 2, lines 23-24, the Office Action admits that "Wilson fails to teach the reference signal being characterized by a constant predetermined frequency" as specified by claim 1, but on page 2, line 25 through page 3, line 1, the Office Action asserts "Janc et al [Janc] teaches these features, the reference quadrature signal from [sic.] 1976, LO 626 in Fig. 6, is characterized by the clock 1934 of a constant predetermined frequency to generating reference signal cos $2\pi fcnT$/sin $2\pi fcnT$ from a clock signal to 644 in Fig. 6]." The Office Action on page 3, lines 9-11, asserts "it would have been obvious to place" Wilson's analog "components 18, 22, 24, 24, 35 [i.e., processing circuitry] into the processor of Wilson & Janc that produces the references signal."

Although ambiguous as stated above, this statement might be used to argue that Janc discloses some form of processor. Therefore, because the Office Action is ambiguous as to how the processing circuitry is supposed to be implemented in "the processor of Wilson & Janc that produces the references signal," a complete response to the Office Action requires a discussion of the error in this position. If the Patent Office did not mean to propose implementing processing circuitry in "the processor of Wilson & Janc that produces the references signal," the Patent Office is invited to clarify its position in its next responsive communication. In the mean time, the error in this position is discussed below.

Since the claims at issue are apparatus claims, the Office Action's use of the phrase "these features" (apparently referring to "reference signal being characterized a constant predetermined frequency") is still ambiguous as to what structure from Janc's patent is being proposed to satisfy the claim limitation of a processor that provides the constant frequency reference signal. A disembodied reference signal from Janc's LO 626 makes no sense in an apparatus claim unless the structure producing the reference signal is to be regarded as a part of the claimed processor. Does the Office Action propose extracting Janc's LO 626 and inserting it into Wilson as the claimed processor? How much of Janc's disclosed structure is to be regarded as "the processor?"

Janc discloses a digital signal processor, a DSP, wholly separate and distinct from the digital zero-IF selectivity section (DZISS), although the DZISS is coupled to the DSP. Janc also discloses that the separate and distinct DZISS includes a direct digital synthesizer (DDS) described in Janc as digital quadrature local oscillator 626 (see Janc column 10, lines 37-44 and column 20, lines 57-60). Claim 1 specifies "a processor and an RF bridge coupled ... to receive a reference signal from the processor." What structure, disclosed by Janc, is to be regarded as "the processor?" Below are listed the five of the most likely candidates. The Patent Office is invited

to clarify how much of the structure disclosed by Janc is to be regarded as the processor in the next responsive communication.

i. First, the claimed processor might be interpreted to be Janc's digital quadrature local oscillator 626 of FIG. 6 (a DDS) all by itself. In such a case, this proposed modification of Wilson's circuit would be to pluck Janc's digital quadrature LO 626 (or 426 or 1926) out of Janc's circuitry and drop it into Wilson's circuitry as a replacement for Wilson's low frequency oscillator 18.

However, this interpretation is incompatible with the express disclosure of Janc. Janc discloses that the digital zero-IF selectivity section (DZISS), that includes digital quadrature local oscillator 626 of FIG. 6, is coupled to but distinct from a digital signal processor, a DSP (see Janc column 10, lines 37-44 and column 20, lines 57-60). In light of Janc's express disclosure of a DSP, digital quadrature local oscillator 626 all by itself cannot be regarded as "the processor" of claim 1, and the RF bridge circuitry cannot be regarded as receiving the reference signal from "the processor." Janc's digital quadrature local oscillator 626 is not a processor; it's a DDS.

Furthermore, Janc's digital quadrature LO 626 (or 426 or 1926) plucked out of Janc's circuitry and dropped into Wilson's circuitry as a replacement for Wilson's low frequency oscillator 18 would not work. The digital word outputs of digital quadrature oscillator 626 are incompatible with the analog signal input to the analog RF bridge (asserted to be Wilson's 4, 5, 6, 14, 10, 20 and 12). This incompatibility, among other reasons, would negate any motivation that a person of ordinary skill in the art might otherwise have for making the proposed substitution without further modifications. M.P.E.P., section 2143.01, instructs that there is no suggestion or motivation to make a proposed modification when the modification renders the prior art invention (in this case, Wilson) unsatisfactory for its intended purpose. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)." Therefore, even with Wilson's analog low frequency oscillator 18 were to be replaced with Janc's digital quadrature local oscillator 626 of FIG. 6 (or 426, or 526, or 1926), Janc's DDS by itself does not constitute "the processor."

ii. Second, the claimed processor might be interpreted to be solely Janc's DSP. However, with such an interpretation the claimed reference signal that the Office Action asserts to be the output of digital quadrature local oscillator 626 cannot be said to come from the "processor" as specified in claim 1 since the digital quadrature local oscillator 626 (a DDS) is part of the DZISS that is outside of the DSP.

iii. Third, the claimed processor might be interpreted to be Janc's digital zero-IF selectivity section (DZISS) all by itself, such as DZISS 1920. The Office Action, on page 4, lines 8-11, in a section discussing claims 9 and 27, asserts "Janc teaches the processing circuitry including a digital frequency source to generate a reference signal based on a signal from a clock source [the processor circuit 1920 includes a digital source generator 1976, LO 626, to generate reference quadrature signal from clock source 1934, Fig. 6, col. 11, lines 12-

23 & col. 12, lines 1-60]" (brackets in original). It would appear that the Office Action is asserting that the processor includes the whole of the DZISS, not just a DDS, since 1920 is DZISS 1920. Contrary to the Office Action's erroneous assertion that 1920 is a processor circuit, Janc's column 20, line 43, disclosure refers to 1920 as DZISS 1920, a digital zero-IF selectivity section (also see column 9, lines 55-56), and not as a processor circuit. Janc's FIG. 19 discloses "a block diagram of a receiver employing the digital zero-IF selectivity section of FIG. 4" (column 6, lines 12-13). This is a specific digital implementation of digital mixers, digital local oscillators and digital filters. In contrast, Janc's disclosure is that his structure includes a separate processor referred to as a digital signal processor, DSP (see Janc column 10, lines 37-44 and column 20, lines 57-60). The Office Action's referring to the DZISS as a processor circuit mischaracterizes, and is contrary to, the disclosure of Janc.

iv. Fourth, the claimed processor might be interpreted to be the DSP plus the whole of the DZISS disclosed by Janc. This is suggested by the Office Action's assertions on page 4, lines 8-11 of "the processor circuit 1920 ..." since 1920 is disclosed as a DZISS. However, the Office Action does not cite any teaching or suggestion that would lead, or even assert reasoned argument that would motivate, an ordinarily skilled person to pick and choose this specific combination of a DSP and a DZISS.

Even if, *arguendo*, an artificial line were to be drawn around Janc's DSP and the entirety of Janc's DZISS including both the digital quadrature LO 626 (or 426 or 1926) and digital mixers (422, 424 of FIG. 4 or 1922, 1924 of FIG. 19), and all circuits within were to be regarded as a processor, Wilson in view of Janc still does not disclose, teach or suggest "an RF bridge coupled to the processor to receive a reference signal from the processor" (emphasis added) as specified in claim 1. Digital quadrature LO 626 (or 426 or 1926) provides its output to digital mixers within the DZISS. If the DZISS were regarded as part of the processor, the output of digital quadrature LO 626 would be internal to the DZISS and only coupled to the digital mixers. Any reference signal output from the digital quadrature LO 626 is not output from "the processor" without further modification of Wilson in view of Janc. Since the digital mixers (422, 424 of FIG. 4 or 1922, 1924 of FIG. 19) within the DZISS cannot be regarded as a part of both the claimed processor and the claimed RF bridge at the same time, Wilson in view of Janc does not disclose, teach or suggest that the claimed reference signal is received by the RF bridge.

v. Fifth, the claimed processor might be interpreted to be Janc's DSP plus the direct digital synthesizer (DDS) disclosed by Janc in FIG. 6 but not the remaining parts of a DZISS such as DZISS 1920. However, the Office Action does not cite any teaching or suggestion that would lead, or even assert reasoned argument that would motivate, an ordinarily skilled person to pick and choose this specific combination of a DSP and a digital quadrature LO 626.

Even if, *arguendo*, an artificial line were to be drawn around Janc's DSP and just Janc's digital quadrature LO 626 (or 426 or 1926), and all circuits within the artificial line were to be regarded as a processor, Wilson in view of Janc still does not disclose, teach or suggest "an RF bridge coupled to the processor to receive a reference signal from the processor" as specified in claim 1. Instead, Janc would then be disclosing a processor in which a DDS (626 of FIG. 6) of

the processor is connected to a pair of digital mixers in a separate down converter (or up converter) that Janc calls a DZISS. Without further modification, Janc only discloses sending the output of the DDS to a separate down converter (or up converter). Janc does not disclose sending the output of the DDS to an outside circuit (e.g., RF bridge) as a reference signal.

c. Responding To The Office Action's Rejection Of Claim 1.

The Office Action's rejection of claim 1 appears to be based on modifying the circuit of Wilson to replace the signal from Wilson's low frequency oscillator 18 with a digital reference signal described in Janc but disembodied from any structure (e.g., Janc's digital quadrature local oscillator 626) that produces the digital reference signal, placing it all in control unit 88 of Weckstrom since control unit 88 is asserted to be a processor and then adding back the structure of Janc's 626 that produces the digital reference signal into control unit 88 of Weckstrom. It seems more straightforward to argue to implement Wilson's analog processing circuitry digitally in Weckstrom's control unit 88, and then modify this combination to include Janc's digital quadrature local oscillator 626 to produce the reference signal, but this is not the Office Action's position.

In either case, the Office Action fails to establish a *prima facie* case for the obviousness of claim 1, at least because it fails to cite references that disclose the structure of the claimed invention or that teach sufficiently to have motivated a person of ordinary skill in the art at the time of the invention to make the modification to Wilson asserted in the Office Action to have been obvious.

i. Even if, *arguendo*, both Janc was to be regarded as analogous prior art sufficient to have been commended to the attention of the inventor, Wilson in view of Janc and/or Weckstrom does achieve the structure of the claimed invention. As discussed throughout this brief, the Office Action asserts that Janc's digital quadrature LO 626 is at least part of one processor that generates the claimed reference signal and Weckstrom's control unit 88 is a second processor that receives the information signal. Claims 1-2, 9, 14-15, 24 and 27 specify only a signal processor.

The Office Action argues that Weckstrom's control unit 88 is the processor into which all circuitry is placed. On page 3, line 5, the Office Action admits, "Wilson & Janc fail to teach placing the above modified circuitry into a processor." However, the Office Action then asserts, on page 3, lines 6-9, that "Weckstrom teaches the control unit 88, Fig. 5, for processing the information signal received from filter 86 for the antenna direction control having A/D converter 92 & associated functional blocks; the reference clock 104 for generating synchronization reference signal to 98, 102 [col. 9, line 45 to col. 10, line 34]" (brackets in original).

It now appears that the Office Action is attempting to assert that a reference clock signal from Weckstrom's clock block 104 is the claimed reference signal instead of the output of Janc's digital quadrature LO 626. This changes the Office Action's earlier assertion that Janc's digital quadrature LO 626 is one processor that generates the claimed reference signal coupled to the RF bridge (Office Action page 3, lines 2-4) to a later assertion that Weckstrom's control unit 88 is

another processor that generates a reference clock signal from clock block 104. However, in this later assertion, the reference clock signal from clock block 104 in Weckstrom's control unit 88 is not coupled to the claimed RF bridge as specified in claim 1. Furthermore, Janc's digital quadrature LO 626 cannot be substituted to replace Weckstrom's clock block 104, under the rubric of placing the components of Wilson & Janc in a processor, at least because Weckstrom's counter 98 would no longer work if its clock signal were to come from the output of Janc's digital quadrature LO 626, and this would negate any motivation to make the substitution.

Because Weckstrom suggests control unit 88 is at least partly a digital processor since it includes ADC 92, a question is raised as to whether the DSP of Janc (and either DDS 626 or DZISS 1920) is to be replaced by or augmented by control unit 88 of Weckstrom, *vice versa*, or whether the two are to remain separate. The Office Action doesn't say.

Weckstrom discloses two main embodiments. The first disclosed embodiment includes receiver 90, control unit 88, antenna unit 52, amplifier 84 and filter 86. Receiver 90 is depicted in summary in FIG. 5 but depicted in detail in FIG. 4. Control unit 88 is depicted in summary in FIG. 4 but depicted in detail in FIG. 5. The signal from receiver 90 passes through amplifier 84 and filter 86, is converted to digital in ADC 92 and filtered in filters 94, 96.

The Office Action asserts that reference clock 104 is for generating synchronization reference signal to 98, 102. This assertion is respectfully traversed as being contrary to the disclosure of Weckstrom.

Weckstrom's component 102 is disclosed as a block to separate the synchronizing signal from its carrier signal (column 10, lines 11-13), to modulate an output signal from control unit 88 (the output of a direction finder is a bearing angle) onto a clock signal carrier (column 10, lines 13-18), and transfer the synchronizing signal from block 102 to clock block 104 (column 10, lines 18-20). Although Weckstrom is not very clear, it appears that clock block 104 operates as a clock generator synchronized by the synchronizing signal from block 102 (column 10, lines 20-22). This might suggest some form of VCO in a phase-locked loop. Weckstrom's text is quite clear that the clock signal from block 104 controls counter 98 (column 10, lines 22-23); however, FIG. 5 regrettably shows an arrow pointing the wrong way.

In any event, Janc and Weckstrom disclose two different processors, not one processor as specified in present claim 1.

ii. The Office Action fails to establish a *prima facie* case for the obviousness of claim 1, at least because it fails to cite evidence, or advance reasoned argument, of a teaching or suggestion that would have motivated a person of ordinary skill in the art at the time of the invention to have made the specific modification of Wilson that are asserted in the Office Action.

The legal standard is that evidence must show a suggestion, teaching, or motivation to combine the prior art references to establish a *prima facie* case for the obviousness of a claim. "[T]he central question is whether there is reason to combine references," *McGinley v. Franklin*

Sports, Inc., 262 F.3 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001). "[A] showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding'," *Brown and Williamson Tobacco Corp. v. Phillip Morris Inc.*, 229 F.3d 1120, 1124-1125, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000). "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)." See M.P.E.P., section 2143.01, page 2100-98, Rev. 1, Feb. 2000, 7th Ed.

Assertions of Patent Office personnel do not constitute evidence. "[I]t is fundamental that rejections under 35 U.S.C. 103 must be based on evidence comprehended by the language of that section." *In re Grasselli*, 713 F.2d 731, 739, 218 USPQ 769, 775 (Fed. Cir. 1983). For example, substantial evidence of prior art might be identified in a prior art patent. The determination of obviousness under 35 U.S.C. §103(a) is a legal conclusion that must be based on factual evidence. *Burlington Indus., Inc. v. Quigg*, 822 F.2d 1581, 1584, 3 USPQ2d 1436, 1439 (Fed. Cir. 1987). Generally, results of the factual inquires articulated in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966), provide the factual basis upon which the legal conclusion of obviousness can be based. The factual basis includes reasoned findings backed by substantial evidence supporting the reasoned findings. The Office Action does not cite any evidence that would have motivated an ordinarily skilled person to modify Wilson's low frequency oscillator 18 to be more accurate and stable.

Motivation can only be found where the evidence shows a teaching or suggestion of the desirability of the specific modification or combination. "[T]here must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant" (emphasis added), *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed Cir. 1998). "[P]articular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention would have selected these components for combination in the manner claimed," *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). For example, although Janc discloses "Referring now to FIG. 6, digital quadrature LO 626 is depicted in block diagram form. Implementation of a DZISS hinges on the ability to generate accurate and stable discrete time representations of sine and cosine waveforms for the quadrature mixing process" (see column 11, lines 1-5), Janc fails to suggest a reason for specifically replacing Wilson's low frequency oscillator 18 with Janc's DDS.

First, replacing Wilson's analog oscillator 18 with Janc's DDS 626 would not work without significant additional modification to couple digital output words from a direct digital synthesizer to an analog phase lock loop. The Office Action, on page 2, lines 23-24, admits that "Wilson fails to teach the reference signal being characterized by a constant predetermined frequency" as specified by claim 1; however, on page 2, line 25 through page 3, line 1, the Office Action asserts "Janc et al [Janc] teaches these features, the reference quadrature signal from [sic.] 1976, LO 626 in Fig. 6, is characterized by the clock 1934 of a constant predetermined frequency to generating reference signal cos $2\pi fcnT$/sin $2\pi fcnT$ from a clock signal to 644 in Fig. 6]." The Office Action fails to establish that replacing Wilson's oscillator 18 with Janc's digital quadrature local oscillator 626 would even work for the Office Action's asserted purpose without substantial further modification to Wilson. M.P.E.P., section 2143.01, instructs that there is no

suggestion or motivation to make a proposed modification when the modification renders the prior art invention (in this case, Wilson) unsatisfactory for its intended purpose. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)." Furthermore, the required additional modification, at a minimum, would negate any motivation for so modifying Wilson.

Second, Wilson in view of Janc does not disclose, teach or suggest any reason why a person of ordinary skill in the art would be motivated to pluck Janc's digital quadrature LO 626 (or 426 or 1926 or whatever structure is ultimately regarded as the processor of Janc) out of Janc's circuitry and drop it into Wilson's circuitry as a replacement for Wilson's low frequency oscillator 18. As discussed above in section 2(b), the Office Action's assertion as to what part of Janc's disclosed circuitry is to be regarded as the "processor" is ambiguous. For at least the reasons discussed above, there is no motivation to extract any specific one of the several choices of combinations of circuitry from Janc and call it "the processor."

Third, even though the Office Action, on page 3, lines 2-4, asserts that "it would have been [obvious] for one of ordinary skill in the art at the time of invention to upgrade Wilson with Janc's accurate local oscillator signals, in order to provide accurate, stable, local oscillator signal to Wilson as suggested by Janc," the applied art does not disclose, teach or suggest that Wilson's low frequency oscillator needs to be, or would even benefit from being, more stable and accurate. Stability and accuracy are characteristics of a DDS, not motivation to replace Wilson's oscillator 18. Neither Wilson nor Janc admit any deficiency in Wilson's circuitry that would motivate a person of ordinary skill in the art to think that Wilson's oscillator 18 needed to be more accurate and/or stable. In fact, Wilson's circuit would still function fine if analog low frequency oscillator 18 were to operate at a slight but significantly different frequency (i.e., poor accuracy) or were to vary slightly but significantly over time (i.e., poor stability) from the design frequency. Accuracy and stability is a characteristic of a DDS, not a motivation for modifying Wilson's circuitry to include a DDS. Assertions of characteristics of a DDS (i.e., accuracy and stability), without more, is not assertions of a motivation for modifying Wilson as specifically proposed.

There is no reason to even want to make this specific substitution. In fact, as can be seen in Janc's FIG. 6, Janc's DDS is a rather complicated structure. In contrast, Wilson's low frequency oscillator 18 could be made much simpler and more cheaply. The complexity difference between a DDS (e.g., Janc's FIG. 6) and Wilson's analog low frequency oscillator 18 is sufficient, by itself, to negate any motivation for the proposed modification. In addition, the incompatibility of the digital circuits of a DDS with the analog circuits of the claimed RF bridge would further negate motivation for the proposed modification. There is nothing in Wilson or Janc that would suggest any benefit (i.e., motivation) would be had by this substitution.

Fourth, the applied patent references do not suggest the motivation asserted in the Office Action (i.e., "to integrate the circuitry components into a processor I.C."). On page 3, lines 10-13, the Office Action asserts that "it would have been obvious to place components 18, 22, 24, 26, 35 into the processor of Wilson & Janc that produces the references signal, in order to

integrate the circuitry components into a processor I.C. together with software accuracy & reduced circuitry size, less signal delay, to increase the processing speed." This assertion makes no sense. The "components 18, 22, 24, 26, 35" are analog components of Wilson. It must be assumed that the Office Action is trying to assert that the functions of analog components 18, 22, 24, 26, 35 are to be implemented in whatever structure of Janc is to be regarded as the claimed "processor." Presumably, the Janc processor is Janc's DSP plus either DDS 626 alone or all of DZISS 1920.

Alternatively, by trying to reconcile the Office Action's assertions in page 3, lines 6-9 with the assertions in page 3, lines 10-13, it might also be that the Office Action is trying to assert that the functions of analog components 18, 22, 24, 26, 35 are to be implemented in Weckstrom's control unit 88, if one substitutes Weckstrom for Wilson & Janc in the assertions on page 3, lines 10-13; however, this is contrary to what the Office Action expressly asserts. The Office Action is simply unclear as to what structure is being proposed. The Office Action is so devoid of any clearly stated proposed structure that it cannot be responded to adequately as written.

In either event, the Office Action's asserted motivation "in order to integrate the circuitry components into a processor I.C. together with software accuracy & reduced circuitry size, less signal delay, to increase the processing speed" is not the kind of motivation to make the specific modification necessary for a *prima facie* case of obviousness for combining the teachings of references. The applied art does not disclose, teach or suggest even that it would have been possible to implement the functions of analog "components 18, 22, 24, 26, 35" of Wilson in an I.C. at the time of the invention. For example, the DDS depicted in Janc's FIG. 6 includes a lot of circuitry, and the Office Action fails to cite any evidence that even the DDS alone could be implemented within a single I.C., and certainly fails to cite evidence that the DDS plus all of the other circuitry needed for the proposed modified Wilson circuit could be implemented in a single I.C. Motivation of this kind must be shown by evidence that would support the capability to make the combination. Office Action assertions of unknown authority are not evidence. Absent the capability "to integrate the circuitry components into a processor I.C.," the Office Action's asserted motivation dissolves.

Fifth, the applied art does not disclose, teach or suggest any motivation for the Office Action's proposal to split up the components of Wilson's phase lock loop and implement only a portion of them in a digital processor. Wilson's VCO 16, beat detector 31, filter 33 and phase detector 35 collectively constitute a phase-locked loop (PLL) that generates a local oscillator signal coupled to mixer 14. This local oscillator signal is formed from the high frequency oscillator 8, but offset in frequency by the frequency of low frequency oscillator 18. The Office Action proposes to implement the functions of analog low frequency oscillator 18 and analog phase detector 35 in a processor (supposedly control unit 88 of Weckstrom, but possibly Janc's digital quadrature local oscillator 626, the Office Action is unclear) and leave the rest as analog circuits. The proposal is to split up the PLL and implement part of it digitally and part of it in analog circuits. The applied art includes no teaching that a portion of the PLL (phase detector 35) is to be digitally implemented, but the remaining parts are to remain analog. Furthermore, to even work, there would be a need to insert either a suitable analog to digital converter or a digital

to analog converter at interfaces between the analog and digital domains. The M.P.E.P., in section 2143.02, instructs that the teachings of the references are not sufficient to render the claims *prima facie* obvious when the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principal under which the [primary reference] construction was designed to operate." "If the proposed modification or combination of the prior art would change the principal of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious," citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

iii. The Office Action's proposal is an exercise in hindsight. The Office Action proposes to modify Wilson's circuitry by replacing Wilson's oscillator 18 with a DDS. The present application discloses that a direct digital synthesizer (DDS) may be used to provide the reference signal. As disclosed in the specification, at page 6, lines 22-24, "the frequency of processor reference signal 202 is based on a direct digital synthesizer, a frequency multiplied replica of a crystal oscillator, or a phase locked loop synthesizer." As disclosed in the specification, at page 9, lines 26-27, "frequency source 206 and DAC 208 constitute a direct digital synthesizer."

Having once learned from the present application that the reference signal may come from a DDS, a search is made to find a DDS disclosed in a prior art reference. DDS circuits are of an accurate and stable character. Then, the Office Action asserts that one would be motivated to modify Wilson with a DDS because a DDS is accurate and stable. This is classic hindsight. Without hindsight, a person of ordinary skill in the art at the time of the invention would not look to Janc to suggest how to design Wilson's low frequency oscillator 18. In fact, Wilson and Janc are not even attempting to solve the same problem. Wilson is an electronic direction finder attempting to locate a bearing angle to a radio emitter. Janc is a radio communication system.

The Office Action improperly imports motivation to make a combination from a non-analogous art references. Remembering that Janc is in a different field of endeavor from the claimed invention, the patent reference and presently claimed invention involve processing different frequencies resulting in different challenges to digital implementations of the functions of analog "components 18, 22, 24, 26, 35" of Wilson in an I.C. The Office Action does not cite any reference that discloses that such different frequencies could be implemented in an I.C. For at least this reason, suggestions of implementing a receiver in a digital processor should not be arbitrarily imported from one field of endeavor (Janc's communication system) into another field of endeavor such as measuring angle rate to compute a range to an emitter. Such importation of suggestions from one field of endeavor to another can only be explained by hindsight.

Furthermore, compounding one supposition upon another draws one from the improbable to the unsupported and directly into hindsight. With each asserted modification, motivated by questionable or lacking suggestions, it becomes less and less probable that a person of ordinary skill in the art would have made the collective modifications. The only reason that such compound modifications are asserted in the first place is by use of impermissible hindsight.

4. Claim 2 Is Not Rendered Obvious By The Applied Art

Even if, *arguendo*, Janc was to be regarded as analogous art to the present invention, the Office Action still fails to establish a *prima facie* case that claim 2, dependent on claim 1, would have been obvious to a person of ordinary skill in the art at the time of the invention. The rejection of claim 2 is respectfully traversed for at least the reasons discussed above with respect to the patentablity of claim 1.

Furthermore, Wilson in view of Janc and Weckstrom does not disclose, teach or suggest:

> a receiver [that] compris[es] a processor and an RF bridge coupled to the processor to receive a reference signal from the processor, the reference signal being characterized by a constant predetermined frequency,
>
> the RF bridge comprising ... a third frequency converter,
>
> wherein the third frequency converter provides an information signal that is coupled to the processor,

as specified in claim 2, dependent on claim 1.

Janc and Weckstrom disclose two separate and distinct processors. Janc discloses a DSP (with either digital oscillator 626 or DZISS 1920) as discussed above. Weckstrom discloses control unit 88 as discussed above. The Office Action is silent as to this distinction. There is no teaching in either reference that these two distinct processors should or could be combined into one. Nevertheless, the Office Action asserts (1) that Janc's processor (in the form of digital quadrature oscillator 626) provides the claimed reference signal and (2) that Weckstom's control unit 88 receives the claimed information signal.

Two distinct processors are contrary to the subject matter specified in claim 2. Claim 1 specifies a receiver including "an RF bridge coupled to the processor to receive a reference signal from the processor." Claim 2 specifies that the "third frequency converter [of the RF bridge] provides an information signal that is coupled to the processor." Claims 1 and 2 specify only one processor, the same processor. The same processor provides the reference signal and the information signal. The references fail to teach this "same processor" feature specified in claim 2.

a. As to Weckstrom: On page 3, lines 6-13, in the section discussing the rejection of claim 1, the Office Action asserts that "Weckstrom teaches the control unit 88, Fig. 5, for processing the information signal received from filter 86 for the antenna direction control having A/D converter 92 & associated functional blocks; the reference clock 104 for generating synchronization reference signal to 98, 102 [col. 9, line 45 to col. 10, line 34]. Therefore, it would have been obvious to place components 18, 22, 24, 26, 35 into the processor of Wilson & Janc that produces the references signal, in order to integrate the circuitry components into a

processor I.C. together with software accuracy & reduced circuitry size, less signal delay, to increase the processing speed." The Office Action asserts that Weckstom's control unit 88 is a first processor that receives the claimed information signal.

b. As to Janc: However, the Office Action argues that it is obvious to modify "the processor of Wilson & Janc that produces the references signal" and "to place components 18, 22, 24, 26, 35 [of Wilson] into the processor." As discussed above, "the processor of Wilson & Janc that produces the references signal," is likely one of (1) solely the DSP disclosed in Janc, (2) the DSP plus the DDS disclosed by Janc and (3) the DSP plus the DZISS disclosed by Janc. The Office Action is ambiguous as to how much of the structure disclosed by Janc is contained in what is to be regarded as "the processor." In any event, the Office Action asserts that Janc discloses a second processor, different than the first processor, to produce the claimed reference signal.

As discussed above, if the processor referred to by the Office Action is construed as just the DSP alone as disclosed by Janc, then the claimed reference signal does not actually come from the processor as specified in claim 1. Alternatively and as discussed above, if the processor referred to by the Office Action is construed as the DSP plus the isolated DDS, the claimed reference signal from the DDS part of the processor is connected to a pair of digital mixers and does not actually connect to the RF bridge as specified in claim 1. As discussed above, if the processor referred to by the Office Action is construed as the DSP plus the DZISS, the claimed reference signal from the DDS is internal to the DZISS part of the processor and does not actually connect to the RF bridge as specified in claim 1.

c. In any event, Weckstrom's control unit 88 is the processor that receives the claimed information signal, and Janc's processor (whatever it is) is the processor that produced the claimed reference signal, but the two processors are not the same processor as specified in claims 1 and 2. Weckstrom alone does not produce the claimed reference signal coupled to the RF bridge, and Janc alone does not receive the claimed information signal from the RF bridge. There is no disclosure or suggestion of combining both into one processor.

5. Claim 24 Is Not Rendered Obvious By The Applied Art

Even if, *arguendo*, Janc was to be regarded as analogous art to the present application, the Office Action still fails to establish a *prima facie* case that claim 24, dependent on claim 1, would have been obvious to a person of ordinary skill in the art at the time of the invention. The rejection of claim 24 is respectfully traversed for at least the reasons discussed above with respect to the patentablity of claim 1.

Furthermore, Wilson in view of Janc and Weckstrom does not disclose, teach or suggest:

> a receiver [that] compris[es] a processor and an RF bridge coupled to the processor to receive a reference signal from the processor, the reference signal being characterized by a constant predetermined frequency,

the RF bridge including first and second frequency converters

wherein the reference signal is coupled to only one of the first and second frequency converters,

as specified in claim 24.

On page 5, the Office Action asserts "[f]or claim 24, Wilson teaches the wherein the reference signal is coupled to only one of the first and second frequency converters [the reference signal from oscillator 16 is only coupled to mixer 14, but not coupled to mixer 6, Fig. 2]." This assertion is respectfully traversed for at least the reasons discussed below.

The Office Action now asserts a different signal to be the claimed reference signal. As discussed above with respect to claim 1, the Office Action originally asserts that the claimed reference signal is the 1 MHz signal output from Wilson's low frequency oscillator 18. Now in claim 24, dependent on claim 1, the Office Action redefines the claimed reference signal to be the output of Wilson's VCO 16. This latter claim construction asserted with the rejection of claim 24 is incompatible with claim construction asserted with respect to claim 1. Since claim 24 specifies the connection to be "the reference signal," it is referring to the same reference signal specified in claim 1. The 1 MHz signal output from Wilson's low frequency oscillator 18 that the Office Action asserts to be the reference signal recited in claim 1 is not the reference signal now asserted in the rejection of claim 24. The reference signal output from Wilson's low frequency oscillator 18 is not coupled to only one mixer.

6. Claims 9, 14-15 & 27 Are Not Rendered Obvious By The Applied Art

The Office Action rejects independent claims 9 and 27 and dependent claims 14-15 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,268,829 to Weckstrom in view of U.S. Patent No. 4,893,316 to Janc et al. This rejection is respectfully traversed.

Even if, *arguendo*, Janc was to be regarded as analogous art to the present application, the Office Action still fails to establish a *prima facie* case that claims 9, 14-15 and 27 would have been obvious to a person of ordinary skill in the art at the time of the invention. Wilson in view of Janc and Weckstrom does not disclose, teach or suggest a receiver that includes an RF bridge and a processor "to receive an information signal from the RF bridge" where the processor includes:

a digital frequency source to generate a reference signal based on a signal from a clock source, the reference signal being coupled to the RF bridge;

and

> circuitry to detect a frequency difference from the information signal based on the signal from the clock source

as specified in claim 9, and therefore, contained in claims 14-15 dependent on claim 9. The claimed "circuitry to detect" uses the same clock source as used in the digital frequency source.

As to claim 27, Wilson in view of Janc and Weckstrom does not disclose, teach or suggest a receiver that includes an RF bridge an a processor "to receive an information signal from the RF bridge" where the processor includes:

> a digital frequency source to generate a reference signal using a signal from a clock source, the reference signal being coupled to the RF bridge;

and

> circuitry to detect a frequency difference from the information signal using the signal from the clock source

as specified in claim 27. The claimed "circuitry to detect" uses the same clock source as used in the digital frequency source.

a. The Office Action's Position Re Wilson

The Office Action, the last line of page 3 through the fourth line of page 4, asserts "[f]or claims 9, 27, Wilson teaches a receiver [Fig. 2, abstract] comprising an rf bridge [antenna 4-5, mixer 6, 14, amplifiers 10, 20 & IF mixer 12] and a processing circuitry [18, 24, 26, 22] coupled to the rf bridge to receive an information signal from the rf bridge [the low pass filter 22 receiving output signal from mixer 12], the reference signal [1 MHz signal from oscillator 18] being coupled to the rf bridge" (brackets in Office Action).

b. Digital Source To Generate A Reference Signal

The Office Action admits that "Wilson fails to teach the processing circuitry including a digital source to generate a reference signal based on a signal from a clock source," but then asserts "Janc teaches the processing circuitry including a digital frequency source to generate a reference signal based on a signal from a clock source [the processor circuit 1920 includes a digital source generator 1976, LO 626, to generate reference quadrature signal from clock source 1934, Fig. 6, col. 11, lines 12-23 & col. 12, lines 1-60], in order to generate accurate, stable local oscillator signal [col. 11, lines 1-5]." This assertion is respectfully traversed for at least the reasons discussed above with respect to the rejection of claim 1, incorporated herein by reference.

c. Weckstrom's Circuitry To Detect Is Not Included In The Processor

On page 4, the Office Action admits "Wilson & Janc fail to teach the circuitry to detect a frequency difference from the information signal based on a reference signal, and the processor," but then asserts "Weckstrom teaches the circuitry to detect a frequency difference from the information signal based on the reference signal [68 detects a frequency difference from signal output from 80, 62, col. 8, lines 15-35], and the processor [the control unit 88, Fig. 5, for processing the information signal received from filter 86 for the antenna direction control having A/D converter 92 & associated functional blocks; the reference clock 104 for generating synchronization reference signal to 98, 102 [col. 9, line 45 to col. 10, line 34]." This assertion is respectfully traversed.

First, the claimed "circuitry to detect" that is specified in claims 9 and 27 is part of the claimed processor. Yet the Office Action asserts (1) that Weckstrom's control unit 88 of FIGS. 4, 5 is the claimed processor, and (2) that Weckstrom's mixer 68 of FIG. 4 is the claimed "circuitry to detect" even though it is not included in control unit 88 (asserted to be the processor). Clearly, Weckstrom does not disclose, teach or suggest that the claimed processor (control unit 88) includes the claimed "circuitry to detect" (mixer 68) as specified in independent claims 9 and 27.

Second, on page 4 the Office Action asserts "it would have been obvious to place components 18, 22, 24, 26, 35 into the processor of Wilson & Janc that produces the references signal, in order to integrate the circuitry components into a processor I.C. together with software accuracy & reduced circuitry size, less signal delay, to increase the processing speed." For at least the reasons discussed above with respect to the rejection of claim 1, this assertion is respectfully traversed.

Accordingly, the rejection of claims 9, 14-15 and 27 is respectfully traversed for at least the reasons discussed.

d. Office Action's Asserted Circuitry To Detect Doesn't Use A Clock Signal

On page 5, the Office Action asserts with respect "to the argument that the circuitry detects from the same clock source," that "since the claim does not recite that the clock source is directly connected to the circuitry, then it is still considered that the circuitry described above is "based on the signal from the clock source." At best, the Office Action is asserting an unsupported belief that the two processors (Janc and Weckstrom) would be driven by the same clock signal. The Office Action assertion is respectfully traversed.

Claims 9 and 27 specify (1) that the single processor includes both the digital frequency source and the circuitry to detect a frequency difference from the information signal, (2) that the digital frequency source generates the reference signal based on a signal from a clock source, and (3) that the circuitry to detect a frequency difference from the information signal detects based on the signal from the clock source, i.e., the same signal from the same clock source used by the digital frequency source.

The Office Action proposes that Janc's digital quadrature local oscillator 626 is the source of the claimed reference signal, and accordingly, the clock signal is depicted as an input into phase accumulator 648 of FIG. 6. Such clock signals are typical in digital systems. On the other hand, the Office Action also proposes (with respect to claims 9 and 27) that Weckstrom's mixer 68 constitutes the claimed circuitry to detect. Mixer 68 has no clocks at all. The Office Action's asserted "circuitry to detect" (asserted to be mixer 68) does not use any clock signal at all, but the claimed "circuitry to detect" is specified in claims 9 and 27 to use the claimed clock signal. Based on the Office Action's asserted interpretation, the circuitry to detect cannot use the same signal from the same clock source used by the digital frequency source, as specified in claim 9 and 27, at least because mixer 68 does not use any clock signal.

e. Weckstrom's Circuitry To Detect Not Synched With The Processor

Alternatively, even if, *arguendo*, claims 9 and 27 were to be construed more consonant with the claim construction asserted in the rejection of claim 1 (i.e., the Office Action's assertion of the processor being Weckstrom's control unit 88 as discussed above), the applied art would not achieve the subject matter of claims 9 and 27. Even if the Office Action were arguing that Janc and Weckstrom would be implemented in one I.C. having a central "clock" and to argue that Weckstrom's clock block 104 produces a clock signal, Weckstrom's clock signal from clock block 104 is not synchronized with the so called central clock that is input into Janc's phase accumulator in FIG. 6. Janc's digital quadrature local oscillator 626 of FIG. 6 (read as the source of the claimed reference signal) is driven by the clock signal depicted as an input into phase accumulator 648 (Janc FIG. 6). On the other hand, Weckstrom's clock block 104 in control unit 88 (Weckstrom FIG. 5) outputs a clock signal synchronized by, or separated in, clock separator and modem 102 from a synchronization signal received from input 100. There is no disclosure anywhere that the sources of these two clocks are the same signal, whether directly or indirectly coupled. Instead, Weckstrom's clock from clock block 104 is derived from a synchronization input that is separated from a carrier signal in a synch separator 102 fed by a signal from input 100 (see Weckstrom FIG. 5 and supporting patent text) in such a way that it varies with respect to any clocking signal used by Weckstrom's control unit 88. The output of Weckstrom's clock block 104 and the clock input to phase accumulator 648 (Janc FIG. 6) are two distinct, separate and unsynchronized clock signals. They are not the same signal from the same clock source as specified in claims 9 and 27 and contained in all claims dependent thereon.

f. Conclusion: One Clock Source

The Office Action summarily dismisses this claim limitation by asserting "it is still considered that the circuit described above is 'based on the signal from the clock source'." (see Office Action page 5, lines 1-3 and page 10, lines 3-6). This Office Action assertion is respectfully traversed for at least the reasons discussed above.

Even if, *arguendo*, the Office Action was attempting to argue that the processor of Janc (whatever it is) uses the same clock source (to generate the clock input to phase accumulator 648, FIG. 6) as the processor constituted by Weckstrom's control unit 88, there is no supporting

evidence for this Office Action contention. The Office Actions assertion of placing them in one I.C. is based on hindsight directed from the applicant's own specification.

Page 24 of the present specification reveals the discovery that the "ability to achieve 20% range accuracy is quite difficult. It is only the use of frequency differencing techniques described herein that it is possible to transfer the frequency difference sensed at antennas 102 and 104 to the digital frequency measuring circuitry that evaluates (A-B)/(A+B)" (emphasis added). These frequency differencing techniques are further explained, for example, on page 26, line 25 through page 27, line 2, the specification discloses that the frequency differencing techniques in the claimed processor include a central clock source, "digital frequency source 206 to generate referenced signal 202 based on a signal from the clock source" (emphasis added), and "circuitry to detect a frequency difference from the information signal based on the signal from the clock source (e.g., circuit parts 230, 240, 260, 270 and 280 of FIG. 4)" (emphasis added) as specified in claims 9 and 27. Furthermore, on page 10, lines 17-20 of the specification the circuit part 230 is disclosed as another "digital frequency source 230 [that] provides a 'local oscillator' signal having a frequency that is the sum [of] the frequency of processor reference signal 204 and an offset frequency." The present specification teaches the new utility that range accuracy is achieved when the digital frequency source and the circuitry to detect are both "based on a signal from the clock source." Stated another way the claimed digital frequency source "provides a 'local oscillator' signal having a frequency that is the sum of the frequency of processor reference signal 204 and an offset frequency." Such frequency differencing techniques provide the present invention with new utility, the accurate measurement of range.

Claims 14 and 15 are dependent on claim 9. For at least the same reasons that claim 9 specifies patentable subject matter, claims 14 and 15 also specify patentable subject matter.

B. Claim 25 Is Not Rendered Unpatentable Under 35 U.S.C. 103(a) For Being Obvious Over U.S. Patent No. 3,816,834 To Wilson In View Of U.S. Patent No. 6,268,829 To Weckstrom.

The Office Action rejects claim 25 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 3,816,834 to Wilson in view of U.S. Patent No. 6,268,829 to Weckstrom. This rejection is respectfully traversed.

Wilson in view of Weckstrom does not disclose, teach or suggest a receiver having a processor providing a reference signal and an RF bridge that includes:

> first and second frequency converters coupled to respective first and second antennas, the reference signal [from the processor] being coupled to only one of the first and second frequency converters"

as specified in claim 25.

The Office Action asserts that Wilson teaches all three of:

1. an RF bridge [antenna 4-5, mixer 6,14, amplifiers 10, 20 & IF mixer 12] coupled to the processing circuitry [18, 22, 24, 26, 35] to receive a reference signals from processing circuitry [receiving 1 MHz reference from 18],

2. a RF bridge including first and second frequency converters coupled to respective first and second antennas [the mixer 6, 14 coupled to antenna 4, 5 respectively],

3. the reference signal being coupled to only one of first and second frequency converters [the reference signal from 16 is only provided to mixer 14, but not for mixer 6, Fig. 2].

This assertion is respectfully traversed. Here in one single claim (claim 25) the Office Action asserts two contrary and inconsistent positions. One position is that the claimed reference signal is the "1 MHz reference from 18," and the other position is that the claimed reference signal is "the reference signal from 16 is only provided to mixer 14." Clearly the same signal cannot be regarded to be both originating in Wilson's low frequency oscillator 18 and also originating in Wilson's VCO 16. As a minimum, attempting to short circuit the two signals together would render Wilson unusable. All of the remarks and arguments with respect to claim 24 above are incorporated herein by reference. The rejection of claim 25 is respectfully traversed.

C. Conclusions

The elements and their relationships specified in the present claims provide the present invention with distinct advantages over the prior art. For example, the claims specify receiver subject matter capable of measuring significantly accurate range to a distant radio emitter in a short time interval. The applied references do not recognize these advantages, and therefore, there is no motivation to modify these applied reference to achieve the claimed invention. Withdrawal of the rejections of all claims are earnestly solicited.

Although this paper asserts specific reasons for finding patentability, this paper should not be construed to mean that other reasons are not available.

For at least the reasons discussed above, it is respectfully submitted that the application is in condition for allowance. Prompt allowance is earnestly solicited.

Respectfully submitted,

Date: November 6, 2006

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VIII. Claims Appendix (37 C.F.R. § 41.37(c)(1)(viii))

The following is a copy of the claims involved in the appeal:

1. A receiver comprising a processor and an RF bridge coupled to the processor to receive a reference signal from the processor, the reference signal being characterized by a constant predetermined frequency, the RF bridge including:

first and second frequency converters coupled to respective first and second antennas; and

a third frequency converter coupled to outputs of the first and second frequency converters.

2. The receiver of claim 1, wherein the third frequency converter provides an information signal that is coupled to the processor.

9. A receiver comprising an RF bridge and a processor coupled to the RF bridge to receive an information signal from the RF bridge, the processor including:

a digital frequency source to generate a reference signal based on a signal from a clock source, the reference signal being coupled to the RF bridge; and

circuitry to detect a frequency difference from the information signal based on the signal from the clock source.

14. The receiver of claim 9, wherein the RF bridge includes:

first and second RF frequency converters coupled to respective first and second antennas; and

a third RF frequency converter coupled to outputs of the first and second RF frequency converters.

15. The receiver of claim 14, wherein:

the first and second RF frequency converters receive respective first and second signals from the respective first and second antennas; and

the third RF frequency converter heterodynes signals from the first and second RF frequency converters to provide a signal that is characterized by a frequency difference modulated onto the reference signal, the frequency difference being a difference between a frequency of the first signal and a frequency of the second signal.

24. A receiver according to claim 1, wherein the reference signal is coupled to only one of the first and second frequency converters.

25. A receiver comprising a processor and an RF bridge coupled to the processor to receive a reference signal from the processor, the RF bridge including:

first and second frequency converters coupled to respective first and second antennas, the reference signal being coupled to only one of the first and second frequency converters; and

a third frequency converter coupled to outputs of the first and second frequency converters.

27. A receiver comprising an RF bridge and a processor coupled to the RF bridge to receive an information signal from the RF bridge, the processor including:

a digital frequency source to generate a reference signal using a signal from a clock source, the reference signal being coupled to the RF bridge; and

circuitry to detect a frequency difference from the information signal using the signal from the clock source.

IX. Evidence Appendix (37 C.F.R. § 41.37(c)(1)(ix))

U.S. Patent No. 3,816,834 to Wilson is of record.

U.S. Patent No. 4,893,316 to Janc et al. is of record.

U.S. Patent No. 6,268,829 to Weckstrom is of record.

U.S. Patent No. 3,090,957 to Albanese et al. is of record.

U.S. Patent No. 3,789,410 to Smith et al. is of record.

U.S. Patent No. 4,704,613 to Albanese et al. is of record.

X. Related Proceedings (37 C.F.R. § 41.37(c)(1)(x))

None.